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April 9, 2004

Commissioner for Patents P.O.Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

| Serial No. 10/798,063 03/11/04 |

Howard Chih-Ho Wang et al.

METHOD FOR FORMING DEVICES WITH MULTIPLE SPACER WIDTHS

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April _, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

TSMC-02-276

- U.S. Patent 6,344,398 to Hsu, "Method for Forming
 Transistor Devices with Different Spacer Width," discloses
 transistor devices on a wafer with different spacer widths.
- U.S. Patent 5,874,330 to Ahn et al., "Method for Fabri-cating Semiconductor Device," describes a method of forming different sidewall thicknesses on gate electrodes in cell and peripheral circuitry regions.
- U.S. Patent 6,248,623 to Chien et al., "Method for Manufacturing Embedded Memory with Different Spacer Widths," discusses embedded DRAM technology in which a three layer spacer consisting of a nitride layer between two oxide layers is formed.
- U.S. Patent 6,316,304 to Pradeep et al., "Method of Forming Spacers of Multiple Widths," describes the formation of two different spacer widths on adjacent transistors.

Sincerely

Stephen B. Ackerman,

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